QUAD SERIAL BACKPLANE DEVICE S2064

FEATURES

- Broad operating rate range (0.7 - 1.3 GHz)
  - 1062 MHz (Fibre Channel)
  - 1250 MHz (Gigabit Ethernet) line rates
  - 1/2 Rate Operation
- Quad Transmitter with phase-locked loop (PLL) clock synthesis from low speed reference
- Quad Receiver PLL provides clock and data recovery
- Internally series terminated TTL outputs
- On-chip 8B/10B line encoding and decoding for four separate parallel 8-bit channels
- 32-bit parallel TTL interface
- Low-jitter serial PECL interface
- Local Loopback
- Interfaces with coax, twinax, or fiber optics
- Single +3.3V supply, 2.3 W power dissipation
- Compact 23mm x 23mm 208 TBGA package

APPLICATIONS

- Ethernet Backbones
- Workstation
- Frame buffer
- Switched networks
- Data broadcast environments
- Proprietary extended backplanes

GENERAL DESCRIPTION

The S2064 facilitates high-speed serial transmission of data in a variety of applications including Gigabit Ethernet, Fibre Channel, serial backplanes, and proprietary point to point links. The chip provides four separate transceivers which can be operated individually or locked together for an aggregate data capacity of >4 Gbps.

Each bi-directional channel provides 8B/10B coding/decoding, parallel to serial and serial to parallel conversion, clock generation/recovery, and framing. The on-chip transmit PLL synthesizes the high-speed clock from a low-speed reference. The on-chip quad receive PLL is used for clock recovery and data retiming on the four independent data inputs. The transmitter and receiver each support differential PECL-compatible I/O for copper or fiber optic component interfaces with excellent signal integrity. Local loopback mode allows for system diagnostics. The chip requires a 3.3V power supply and dissipates approximately 2.3 watts.

Figure 1 shows the S2064 and S2066 in a Gigabit Ethernet application. Figure 2 combines the S2064 with a crosspoint switch to demonstrate a serial backplane application. Figure 3 is the input/output diagram. Figures 4 and 5 show the transmit and receive block diagrams, respectively.

Figure 1. Typical Quad Gigabit Ethernet Application

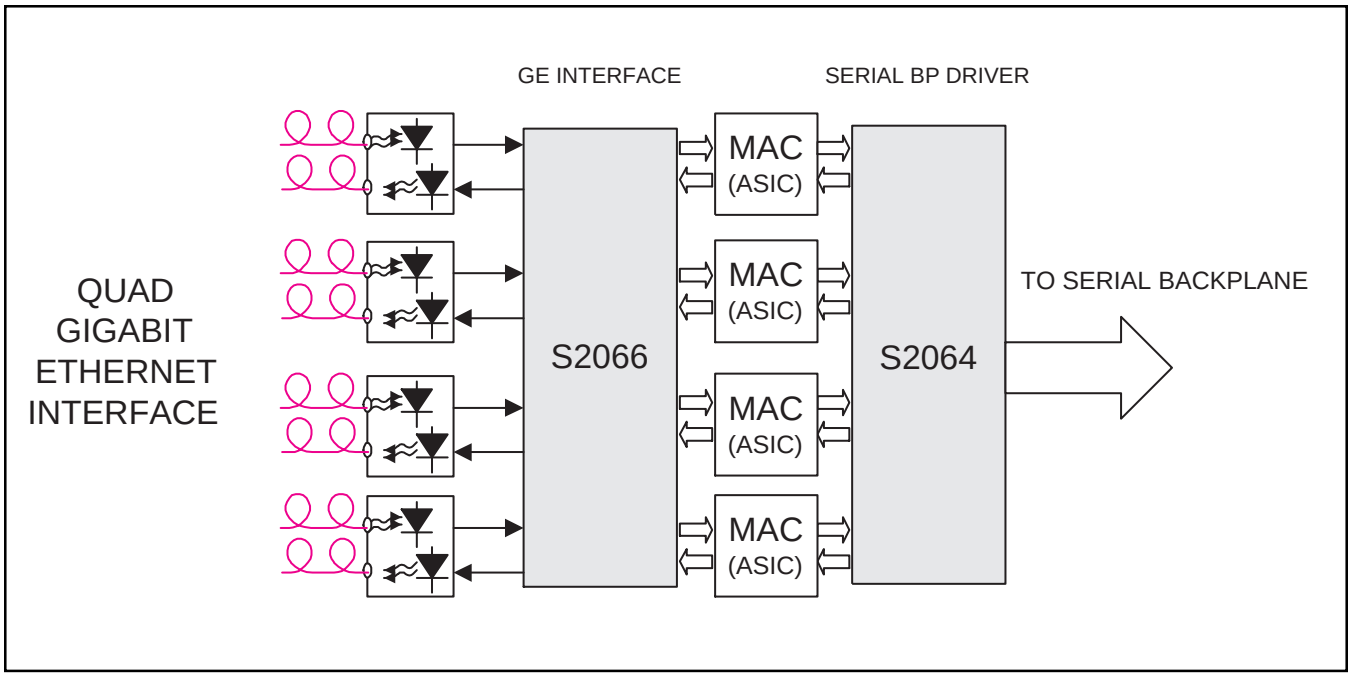


Figure 2. Typical Backplane Application

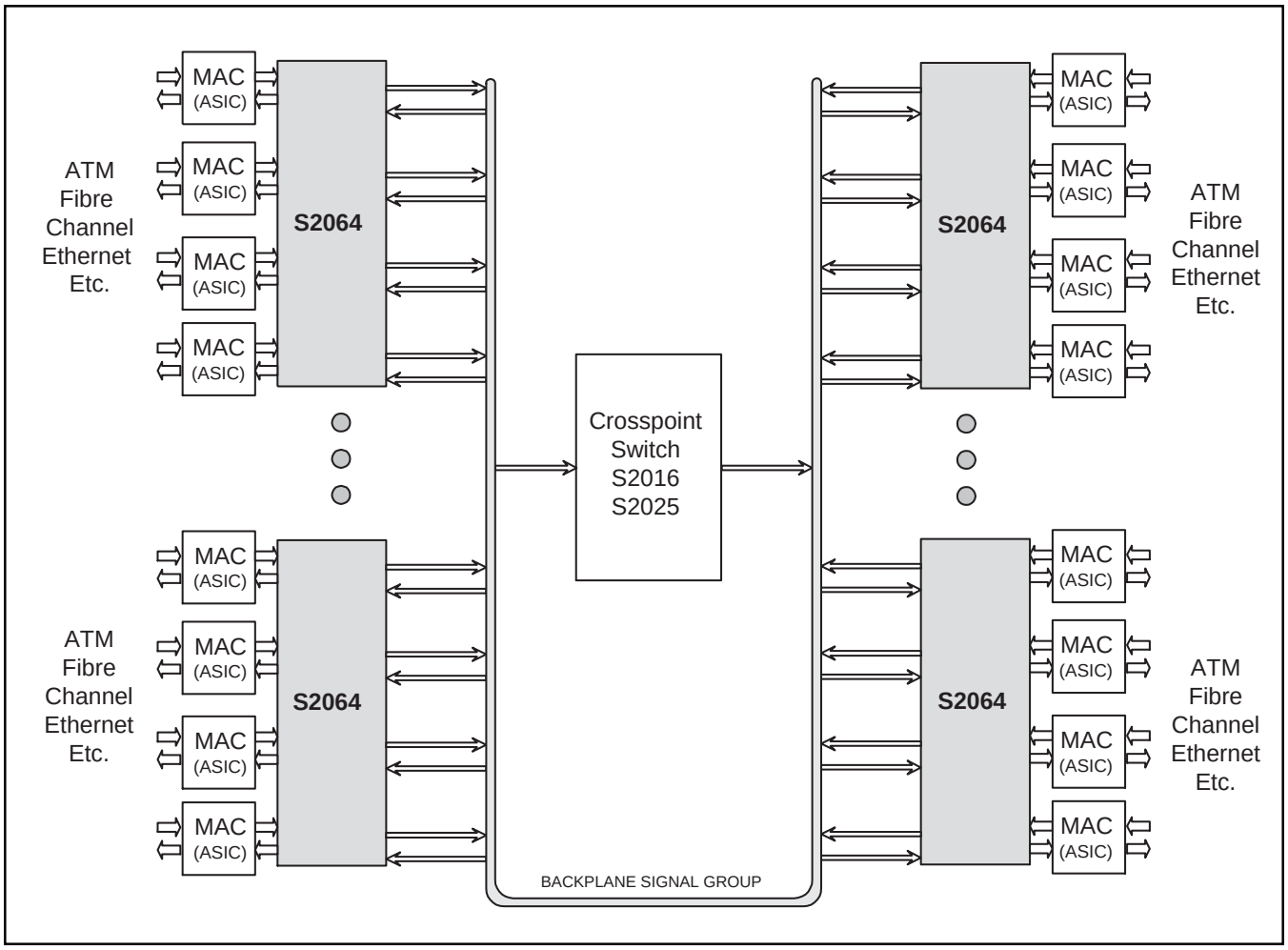


Figure 3. S2064 Input/Output Diagram

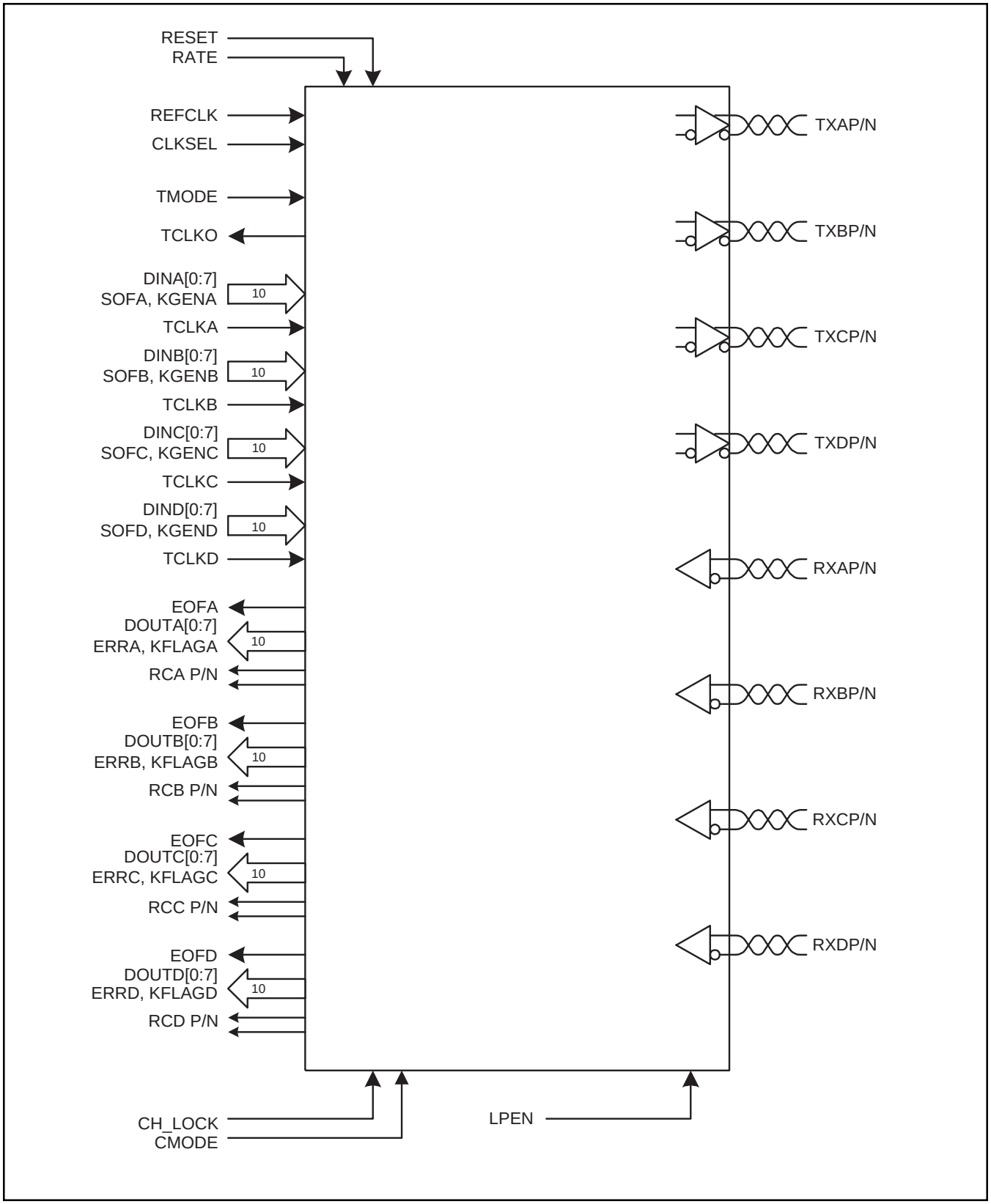


Figure 4. Transmitter Block Diagram

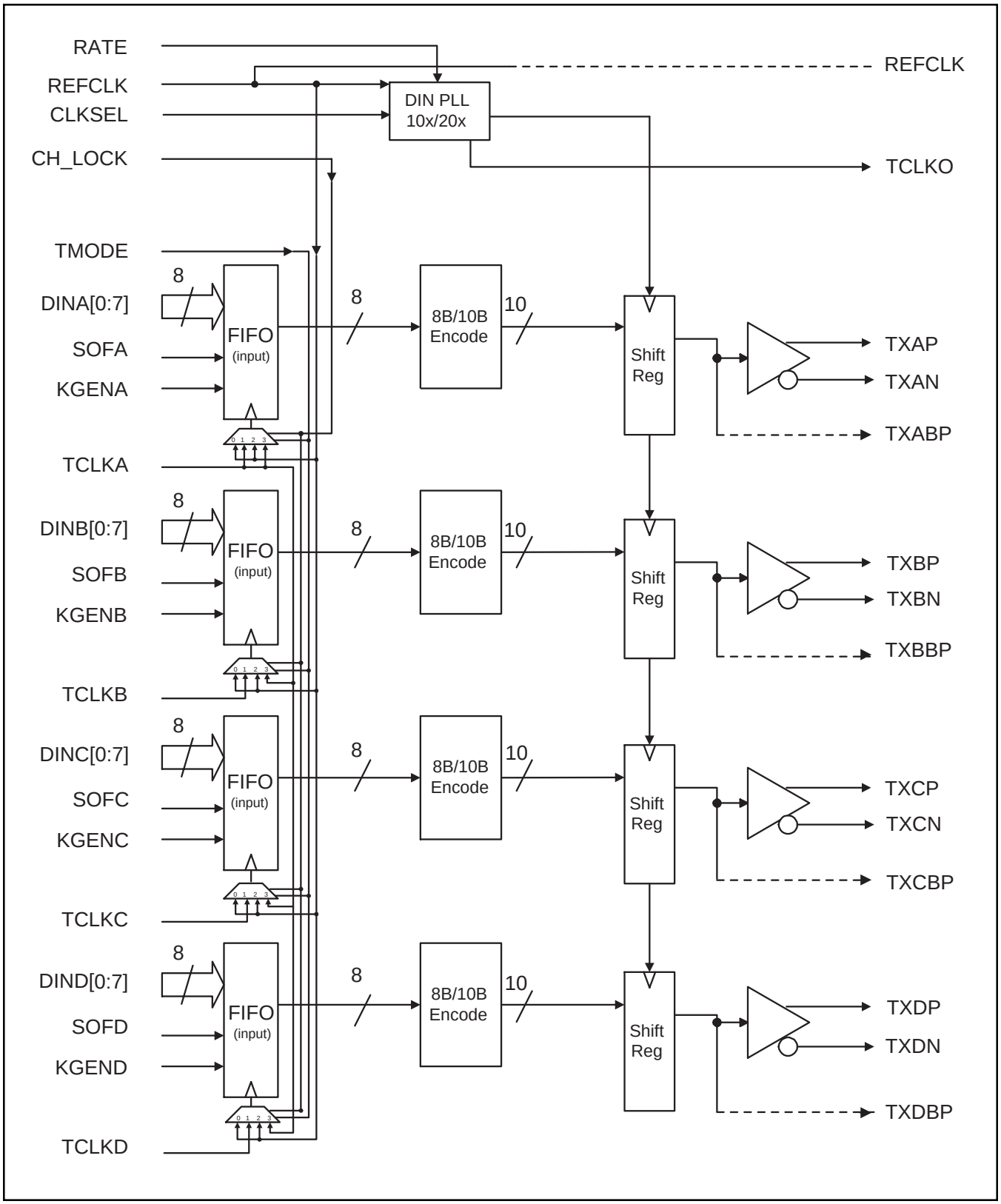
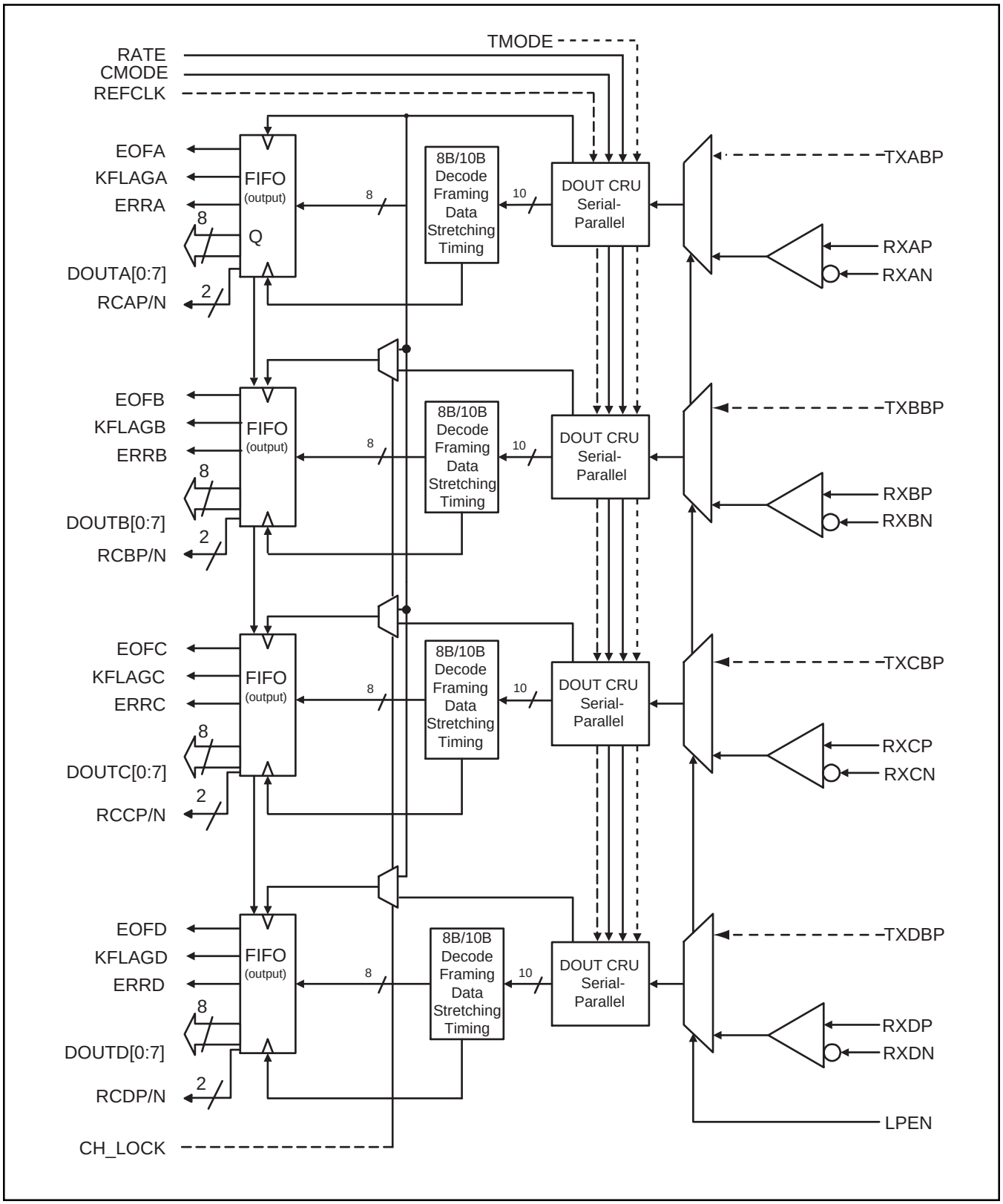


Figure 5. Receiver Block Diagram



TRANSMITTER DESCRIPTION

The transmitter section of the S2064 contains a single PLL which is used to generate the serial rate transmit clock for all transmitters. Four channels are provided with a variety of options regarding input clocking and loopback. The transmitters can operate in the range of 0.77 GHz to 1.3 GHz, 10 or 20 times the reference clock frequency.

Data Input

The S2064 has been designed to simplify the parallel interface data transfer and provides the utmost in flexibility regarding clocking of parallel data. Prior, or less sophisticated, implementations of this function have either forced the user to synchronize transmit data to the reference clock or to provide the output clock as a reference to the PLL, resulting in increased jitter at the serial interface. The S2064 incorporates a unique FIFO structure on both the parallel inputs and the parallel outputs which enables the user to provide a “clean” reference source for the PLL and to accept a separate external clock which is used exclusively to reliably clock data into the device.

Data is input to each channel of the S2064 nominally as a 10 bit wide word. This consists of eight data bits of user data, KGEN, and SOF. An input FIFO and a clock input, TCLKx, are provided for each channel of the S2064. The device can operate in two different modes. In CHANNEL LOCK mode all four bytes of input data are clocked into their respective FIFOs using a common clock. The S2064 can be configured to use either the TCLKA (TCLK MODE) input or the REFCLK input (REFCLK MODE). In NORMAL mode, each byte of data is clocked into its FIFO with the TCLKx provided with each byte. Table 1 provides a summary of the input modes for the S2064.

Operation in the TCLK MODE makes it easier for users to meet the relatively narrow setup and hold time window required by the parallel 10-bit interface. The TCLK signal is used to clock the data into an internal holding register and the S2064 synchronizes its internal data flow to insure stable operation. However, regardless of the clock mode, REFCLK is always the VCO reference clock. This facilitates the provision of a clean reference clock resulting in minimum jitter on the serial output. The TCLK must be frequency locked to REFCLK, but may have an arbitrary but fixed phase relationship. Adjustment of internal timing of the S2064 is performed during reset. Once synchronized, the S2064 can tolerate up to ±3ns of phase drift between TCLK and REFCLK.

Figure 6 demonstrates the flexibility afforded by the S2064. A low jitter reference is q»ovided directly to the S2064 at either 1/10 or 1/20 the serial data rate. This insures minimum jitter in the synthesized clock used for serial data transmission. A system clock output at the parallel word rate, TCLKO, is derived from the PLL and provided to the upstream circuit as a system clock. The frequency of this output is constant at the parallel word rate, 1/10 the serial data rate, regardless of whether the reference is provided at 1/10 or 1/20 the serial data rate. This clock can be buffered as required without concern about added delay. There is no phase requirement between TCLKO and TCLKx, which is provided back to the S2064, other than that they remain within ± 3ns of the phase relationship established at reset.

Table 1. Input Modes

CHANLOCK	TMODE	Operation
0	0	NORMAL REFCLK MODE. REFCLK used for all channels. (No receiver byte de-skew.)
0	1	NORMAL TCLK MODE. TCLKx used to clock data into all FIFOs. (No receiver byte de-skew.)
1	0	CHANNEL LOCK MODE. REFCLK MODE. REFCLK used to clock data into all FIFOs. (Receiver byte de-skew active.)
1	1	CHANNEL LOCK MODE. TCLKA MODE. TCLKA used to clock data into all FIFOs. (Receiver byte de-skew active.)

1. Note that internal synchronization of FIFOs is performed upon de-assertion of RESET.

Figure 6. DIN Data Clocking with TCLK

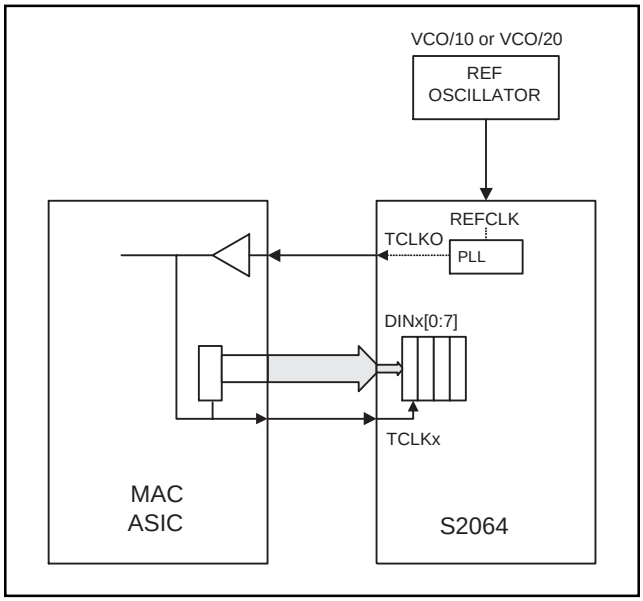
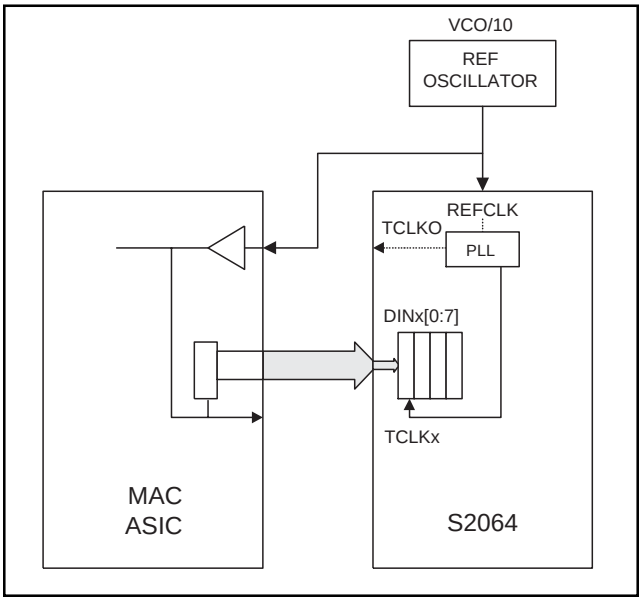


Figure 7. DIN Clocking with REFCLK



The S2064 also supports the traditional REFCLK (TBC) clocking found in Fibre Channel and Gigabit Ethernet application and is illustrated in Figure 7. This approach imposes significant challenges in maintaining timing margins on the designer.

Half Rate Operation

The S2064 supports full and 1/2 rate operation for all modes of operation. When RATE is LOW, the S2064 serial data rate equals the VCO frequency. When RATE is HIGH, the VCO is divided by 2 before being provided to the chip. Thus the S2064 can support Fibre Channel and serial backplane functions at both full and 1/2 the VCO rate.

8B/10B Coding

The S2064 provides 8B/10B line coding for each channel. The 8B/10B transmission code includes serial encoding and decoding rules, special characters, and error control. Information is encoded, 8 bits at a time, into a 10 bit transmission character. The characters defined by this code ensure that enough transitions are present in the serial bit stream to make clock recovery possible at the receiver. The encoding also greatly increases the likelihood of detecting any single or multiple errors that might occur during the transmission and reception of data[1].

The 8B/10B transmission code includes D-characters, used for data transmission, and K-characters, used for control or protocol functions. Each D-character and K-character has a positive and a negative parity version. The parity of each codeword is selected by the encoder to control the running disparity of the data stream. K-character generation is controlled individually for each channel using the KGENx input. When KGEN is asserted, the data on the parallel input is mapped into the corresponding control character. The parity of the K-character is selected to minimize running disparity in the serial data stream. Table 2 lists the K characters supported by the S2064 and identifies the mapping of the DIN[7:0] bits to each character.

A special input, SOF, is provided for each channel to simplify the generation of the K28.5 character. When SOF is asserted, the K28.5 character is generated regardless of the data on the parallel input. The K28.5 character can be of either positive or negative parity, depending on the current running disparity. When the chip is in CHANNEL LOCK mode, assertion of SOFA causes the K28.5 to be generated on all four serial data streams, SOFC is ignored. When SOFD is asserted during CHANNEL LOCK mode, this resets the Channel Lock State Machine. Table 3 shows the mapping of the 8B/10B characters representation. Data is transmitted bit “a” or DIN[0] first.

[1] 1. A.X. Widner and P.A. Franaszek, "A Byte-Oriented DC Balanced (0,4) 8B/10B Transmission Code," IBM Research Report RC9391, May 1982.

In addition to data and K characters, the S2064 can also generate a unique sync sequence consisting of 16 consecutive K28.5 characters. This event is initiated by the simultaneous assertion of KGENx and SOFx for one clock period. The SOFx and KGENx inputs should be held low until the sync sequence has completed. The sync sequence may start with either a positive or negative parity K28.5. (Depending on the current running disparity.) The parity of the second and third K28.5 are inverse with respect to a valid 8B/10B sequence. Parity of the remaining K28.5 alternate in accordance with the 8B/10B coding standard. Thus the parity of the K28.5 pattern consists of + + - - + - + - + - + - + - + - or - - + + - + - + - + - + - + -. Tables 1a and 1b show the transmitter control signals for both Normal and Channel Lock mode.

Frequency Synthesizer (PLL)

The S2064 synthesizes a serial transmit clock from the reference signal. Upon startup, the S2064 will obtain phase and frequency lock within 2500 bit times after the start of receiving reference clock inputs. Reliable locking of the transmit PLL is assured, but a lock-detect output is NOT provided.

Table 1a. Transmitter Control Signals (Normal Mode, CH_LOCK = 0)

SOFx	KGENx	S2064 DIN Output
0	0	Encoded Parallel Data
0	1	K Character as defined by Table 2 and DIN[7:0]
1	0	K28.5 Character
1	1	Special 16 word character, + + - - + - + - + - + - + - + - or - - + + - + - + - + - + - + - +

Table 1b. Transmitter Control Signals (Channel Lock Mode, CH_LOCK = 1)

SOFA	SOFB	KGENx	S2064 Output
0	0	0	Encoded Parallel Data.
0	0	1	K Character as defined by Table 2 on channel x.
1	0	0	K28.5 Character on all four channels.
1	0	1	Special 16 Word Sync Character on channel x.
X	1	X	Special 16 Word Sync Character on all four channels.

Table 2. K Character Generation (SOFx = 0)

K Character	DIN[7:0]	KGEN	Current RD+	Current RD-	Comments
			abcdei fghj	abcdei fghj	
K28.0	000 11100	1	110000 1011	001111 0100	
K28.1	001 11100	1	110000 0110	001111 1001	
K28.2	010 11100	1	110000 1010	001111 0101	
K28.3	011 11100	1	110000 1100	001111 0011	
K28.4	100 11100	1	110000 1101	001111 0010	
K28.5	101 11100	1	110000 0101	001111 1010	Sync Character
K28.6	110 11100	1	110000 1001	001111 0110	
K28.7	111 11100	1	110000 0111	001111 1000	
K23.7	111 10111	1	000101 0111	111010 1000	
K27.7	111 11011	1	001001 0111	110110 1000	
K29.7	111 11101	1	010001 0111	101110 1000	
K30.7	111 11110	1	100001 0111	011110 1000	

Table 3. Data to 8B/10B Alphabetic Representation

	Data Byte									
DIN[0:9] or DOUT[0:9]	0	1	2	3	4	5	6	7	8	9
8B/10B Alphanumeric Representation	a	b	c	d	e	i	f	g	h	j

Reference Clock Input

The reference clock input must be supplied with a low-jitter clock source. All reference clocks in a system must be within 200 ppm of each other to insure that the clock recovery units can lock to the serial data.

The frequency of the reference clock must be either 1/10 the serial data rate, CLKSEL = 0, or 1/20 the serial data rate, CLKSEL=1. In both cases the frequency of the parallel word rate output, TCLKO, is constant at 1/10 the serial data rate. See Table 4.

Table 4. Operating Rates

RATE	CLKSEL	REFCLK Frequency	Serial Output Rate	TCLKO Frequency
0	0	SDR/10	0.77–1.3 GHz	SDR/10
0	1	SDR/20	0.77–1.3 GHz	SDR/10
1	0	SDR/10	0.39-0.65 GHz	SDR/10
1	1	SDR/20	0.39-0.65 GHz	SDR/10

Note: SDR = Serial Data Rate.

Serial Data Outputs

The S2064 provides LVPECL level serial outputs. Each high speed output should be provided with a resistor to VSS (Gnd) near the device. A value of 4.5 KΩ provides optimal performance with minimum impact on power dissipation. The resistance may be as low as 450 Ω, but this will dissipate additional power with no substantive performance improvement. Outputs are designed to perform optimally when AC-coupled.

When operating in the CHANNEL LOCK mode, the user must insure that the path length of the four high speed serial data signals are matched to within 50 serial bit times of delay. Failure to meet this requirement may result in bit errors in the received data or in byte misalignment. In addition to path length induced timing skew, the S2064 can tolerate up to ±3 ns of phase drift between channels after deskewing the outputs.

Test Functions

The S2064 can be configured for factory test to aid in functional testing of the device. When in the test mode, the internal transmit and receive voltage-controlled oscillator (VCO) is bypassed and the reference clock substituted. This allows full functional testing of the digital portion of the chip or bypassing the internal synthesized clock with an external clock source. (See Other Operating Modes section.)

Transmit FIFO Initialization

The transmit FIFO must be initialized after stable delivery of data and TCLK to the parallel interface, and before entering the normal operational state of the circuit. FIFO initialization is performed upon the de-assertion of the RESET signal. The DIN FIFO is automatically reset upon power up immediately after the DIN PLL obtains steady state timing at this point, then the user must initialize by asserting the RESET signal. The TCLKO will operate normally regardless of the state of RESET.

RECEIVER DESCRIPTION

Each receiver channel is designed to implement a Serial Backplane receiver function through the physical layer. A block diagram showing the basic function is provided in Figure 5.

Whenever a signal is present, the receiver attempts to recover the serial clock from the received data stream. After acquiring bit synchronization, the S2064 searches the serial bit stream for the occurrence of a K28.5 character on which to perform word synchronization. Once synchronization on both bit and word boundaries is achieved, the receiver provides the decoded data on its parallel outputs.

The S2064 provides the capability to operate with all four channels locked together (CHANNEL LOCK mode). Channel lock process and status reporting is described below.

Data Input

A differential input receiver is provided for each channel of the S2064. Each channel has a loopback mode in which the serial data from the transmitter replaces external serial data. The loopback function for all four channels is controlled by the loopback enable signal, LPEN.

The high speed serial inputs to the S2064 are internally biased to VDD-1.3V. All that is required externally are AC-coupling and line-to-line differential termination.

Clock Recovery Function

Clock recovery is performed on the input data stream for each channel of the S2064. The receiver PLL has been optimized for the anticipated needs of Serial Backplane systems. A simple state machine in the clock recovery macro decides whether to acquire lock from the serial data input or from the reference clock. The decision is based upon the frequency and run length of the serial data inputs. If at any time the frequency or run length checks are violated, the state machine forces the VCO to lock to the reference clock. This allows the VCO to maintain the correct frequency in the absence of data.

The 'lock to reference' frequency criteria insure that the S2064 will respond to variations in the serial data input frequency (compared to the reference frequency). The new Lock State is dependent upon the current lock state, as shown in Table 5.

Table 5. Lock to Reference Frequency Criteria

Current Lock State	PLL Frequency (vs. REFCLK)	New Lock State
Locked	< 488 ppm	Locked
	488 to 732 ppm	Undetermined
	> 732 ppm	Unlocked
Unlocked	< 244 ppm	Locked
	244 to 366 ppm	Undetermined
	> 366 ppm	Unlocked

The run-length criteria insure that the S2064 will respond appropriately and quickly to a loss of signal. The run-length checker flags a condition of consecutive ones or zeros across 12 parallel words. Thus 119 or less consecutive ones or zeros does not cause signal loss, 129 or more causes signal loss, and 120 - 128 may or may not, depending on how the data aligns across byte boundaries.

If both the off-frequency detect circuitry test and the run-length test are satisfied, the CRU will attempt to lock to the incoming data. When lock is achieved, LOCK-DET is asserted on the ERR, EOF, and KFLAG status lines. It is possible for the run length test to be satisfied due to noise on the inputs, even if no signal is present. In this case the lock detect status may periodically assert as the VCO frequency approaches that of the REFCLK.

In any transfer of PLL control from the serial data to the reference clock, the RCxP/N outputs remain phase continuous and glitch free, assuring the integrity of downstream clocking.

When operating in independent mode, all four PLL lock status is indicated by a 1-0-1 on the ERR, EOF, and KFLAG outputs, respectively. When operating in the CHANNEL LOCK mode, PLL locking of all four channels must be accomplished before byte-skewing is achieved and "In Sync" status is indicated on the ERR, EOF, and KFLAG outputs.

Reference Clock Input

A single reference clock, which serves both transmitter and receiver, must be provided from a low jitter clock source. The frequency of the received data stream (divided-by-10 or -20) must be within 200 ppm of the reference clock to insure reliable locking of the receiver PLL.

Serial to Parallel Conversion

Once bit synchronization has been attained by the S2064 CRU, the S2064 must synchronize to the 10 bit word boundary. Word synchronization in the S2064 is accomplished by detecting and aligning to the 8B/10B K28.5 codeword. The S2064 will detect and byte-align to either polarity of the K28.5. Each channel of the S2064 will detect and align to a K28.5 anywhere in the data stream. Two modes of operation are supported. For NORMAL mode operation, the presence of a K28.5 is indicated for each channel by the assertion of the EOFx signal.

For CHANNEL LOCK operation, the S2064 must provide an additional level of synchronization to insure that differences in delay encountered by the four channels do not result in parallel output data from each channel leading or lagging by one parallel clock cycle. In CHANNEL LOCK, 10 bit mode, assertion of SOFA results in the K28.5 being transmitted simultaneously on all four channels. Each receiver provides a FIFO buffer and adjusts the delay through this buffer to insure that the first data following the K28.5 is output simultaneously from the receiver on the parallel interface. The reception of a K28.5 character is indicated on the EOFA signal. Table 6 details the function of the EOF, KFLAG, and ERR pins in status reporting. For CHANNEL LOCK operation, a single output clock, RCAP/N, is provided synchronous with the data. The other RCxP/N clocks will be frequency locked, but will have an arbitrary phase relationship with the data.

Channel Lock Mode Synchronization

Incidental errors occurring in the received data can transform a normal data character into a K28.5 character. To prevent this occurrence from making the channel locking process unnecessarily vulnerable to bit errors, the S2064 implements a channel lock state machine for each channel with linkage between channels to move to the final de-skewed state.

The Channel Lock state diagram is shown in Figure 8. The S2064 powers up in the “No Sync” state. When in the “No Sync” state, each channel of the S2064 is actively searching the received data stream for the occurrence of a K28.5 and will align its demultiplexor to the character when detected, and will enter the “Acquiring Sync” state. K28.5 will be reported on each channel as 0-1-1 (err-eof-kflag). When four or more consecutive K28.5 characters are received on a given channel, the channel will enter the “Re-sync” state as shown in Figure 8. “Re-Sync” state status will not be reported as 1-1-1 until the first valid data character has been received. If all four channels are in the “Re-sync” state and each has received a valid data character within the deskew time of 5 bytes, then the S2064 will channel lock by aligning the data output from each channel such that the first valid data character for each channel is output simultaneously. The device will move to the “In Sync” state and indicate channel lock status by each channel as a 0-1-0. Note that “Re-sync” is reported independently by each channel regardless of the state of the other channels. However, “In Sync” can only be reported when all four channels are in the “In Sync” state and detect a valid data character within the deskew window. The “In Sync” state is reported for each as 0-1-0.

Once the S2064 has entered the “In Sync” state, it will report status but will not alter the relative skew of the output FIFOs. The S2064 will exit the “In Sync” state and move to the “No Sync” state if one of the four CRUs reports a loss of lock, if the 8B/10B decoder observes four consecutive decoding errors, or if the decoder error rate >50% in a block of 16 codewords. The device can also be put in the “No Sync” state by setting SOFD=Low, asserting RESET, or by momentarily de-asserting CH_LOCK signal.

SOFD is used to reset the Channel Lock state machine and provides minimum disruption of the data path.

When not in Channel Lock Mode, the linkage between the four state machines is broken and each channel operates independently.

Loss of Channel Lock will be reported as indicated in Figure 9 and Table 6 by a 1-0-1 on the ERR, EOF, and KFLAG signals, respectively. This is during the “No Sync” state. The status lines will reflect the status of the individual channels and the device will respond to appropriate channel locking sequences and deskew as necessary. Persistence of 1-0-1 status on any channel is indicative of CRU lock failure, most likely resulting from loss of receiver input signal. The device will then respond to the channel locking sequence.

When operating in the Channel Lock Mode, the TCLK[B-D] inputs must be tied low.

Figure 8. Channel Lock State Machine

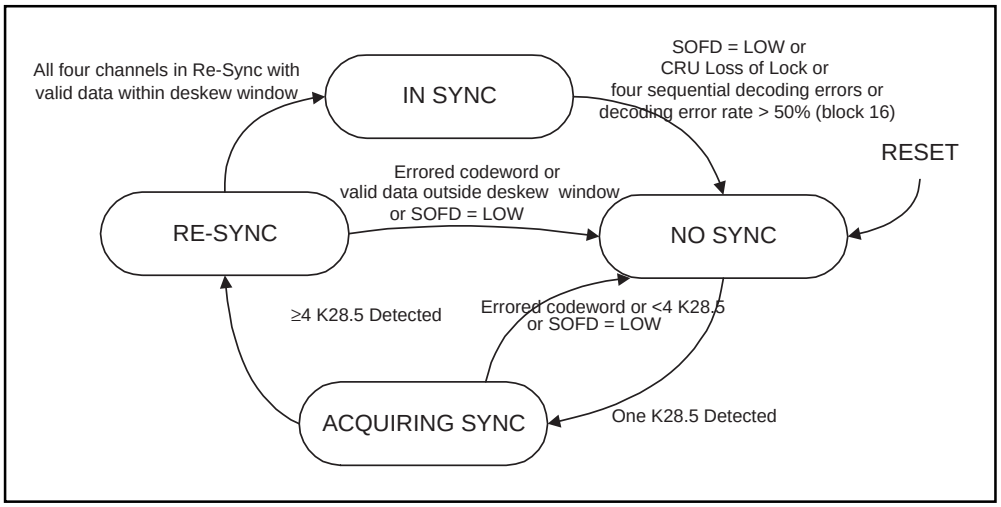
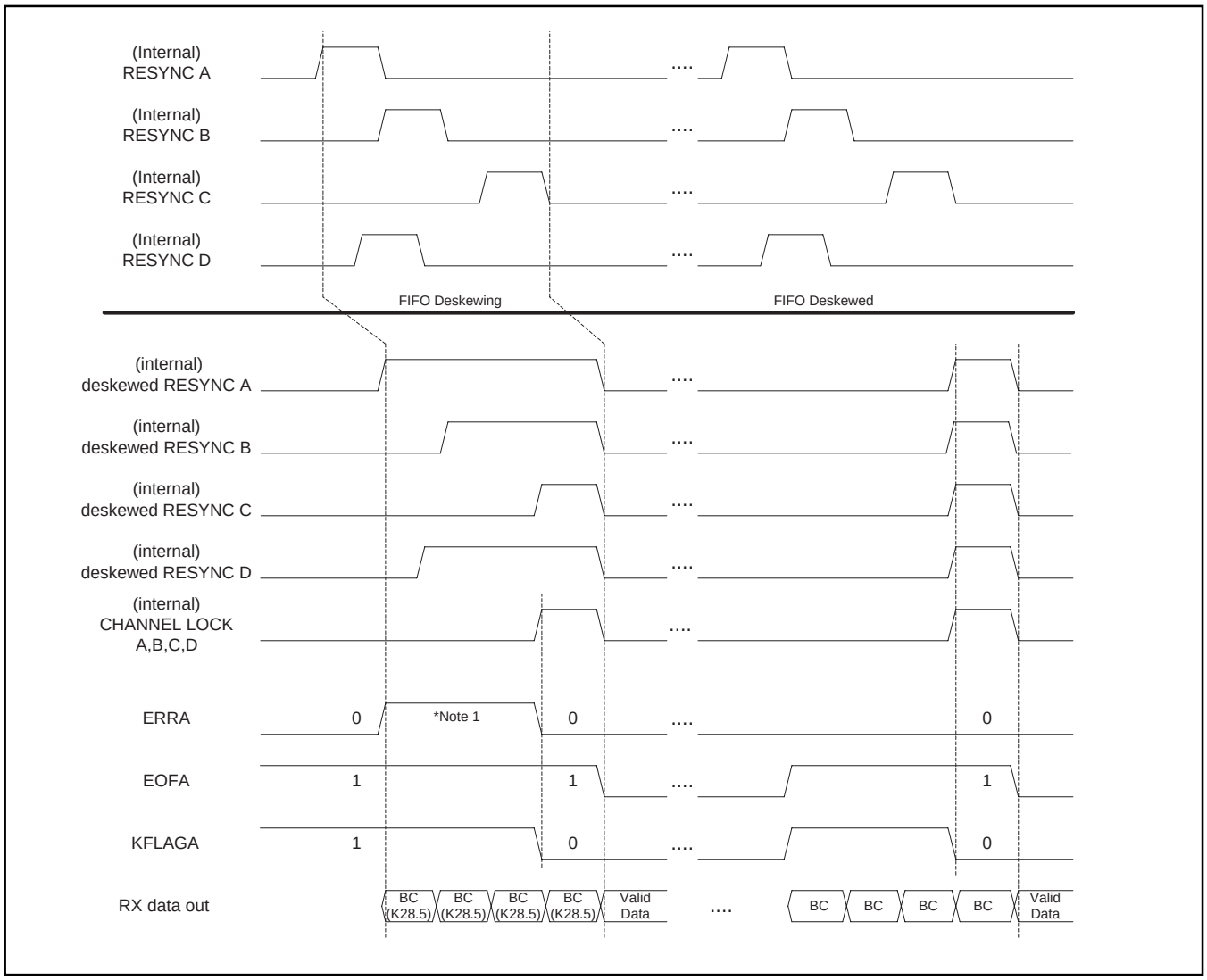


Figure 9. Channel Lock Synchronization Timing



1. The first three K28.5's will be reported as "K28.5" (011), subsequent K28.5 will be reported as "Resync" or "Channel Lock Detected." See Table 6.

Table 6. Error and Status Reporting

ERR	EOF	KFLAG	Description	Rank
0	0	0	Normal Character. Indicates that a valid data character has been detected.	6
0	0	1	K Character (not K28.5). Indicates that a K character other than K28.5 has been detected.	6
0	1	0	Channel Lock Detected. Asserts for one parallel word on the ERRA, EOFA, and KFLAGA signals that all four channels have identified the re-sync sequence within the byte de-skew window.	2
0	1	1	K28.5+ or K28.5-. Indicates that a K28.5 character of arbitrary parity has been detected.	6
1	0	0	Codeword Violation. Indicates that a word not corresponding to any valid Dx.x or Kx.x mapping has been received.	4
1	0	1	Loss of Sync. Asserts for one parallel word to indicate that a condition has occurred which results in loss of channel lock. When operating in the independent mode, indicates loss of CRU bit lock.	1
1	1	0	Parity Error (ignore on K28.5). Indicates that a running disparity error has been observed.	5
1	1	1	Re-Sync (K28.5 x 4 + Dx.x). Asserts for one parallel word indicating that four consecutive K28.5 characters followed by a valid Dx.x character has been received. Each channel reports this condition independently and all four channels must identify the re-sync within the allowed byte de-skew time before channel lock can be achieved and be indicated with CHANNEL LOCK DETECTED (see above).	3

CHANNEL LOCKING/RE-LOCKING PROCEDURE

The Channel locking/relocking procedures are summarized below. Following these procedures will insure proper CHANNEL LOCK operation of the device. When powered up, the S2064 will lock to the received data within approximately 2500 bit times. The CRU must report lock for approximately 32,000 REFCLK periods (320 µs) before channel locking is enabled.

1. Insure that the S2064 is in the "No Sync" state. This can be accomplished by resetting the device by toggling SOFD low, or by de-asserting the channel lock for several clock periods and then re-asserting.
2. Transmit the appropriate synchronization sequence. Four K28.5 characters or the 16 word SYNC sequence can be used to de-skew the DOUT FIFOs. The 16 word SYNC character can be generated by asserting SOFx=1 and KGENx=1.
3. Wait for "channel lock detected" as defined by Table 6.

The S2064 will enter the "No Sync" state if: any CRU loses lock, if the CH_LOCK signal is de-asserted, if four or more consecutive decoder errors are observed, or if the decoder error rate exceeds 50% in a block of 16 bytes, or if SOFD is low. If desired, the CRU lock status of each channel can be checked by de-asserting CH_LOCK and confirming that "Loss of Sync" status (Table 6) is not reported by any channel. To reacquire Sync after moving to the "No Sync" state, repeat steps 2 and 3 above.

8B/10B Decoding

After serial to parallel conversion, the S2064 provides 8B/10B decoding of the data. The received 10-bit codeword is decoded to recover the original 8-bit data. The decoder also checks for errors and flags, either invalid codeword errors or running disparity errors by assertion of the ERRx signal. Error type is determined by examining the EOF output in accordance with Table 6. When more than one reportable condition occurs simultaneously, reporting is in accordance with the rank assigned by Table 6.

Data Output

Data is output on the DOUT[0:7] outputs. K-characters are flagged using the KFLAG signal. The EOF (with KFLAG) is used to indicate the reception of a valid K28.5 character. Invalid codewords and decoding errors are indicated on the ERR output. KFLAG, EOF, and ERR are buffered with the data in the FIFO to insure that all outputs are synchronized at the S2064 outputs. Errors are reported independently for each channel in both CHANNEL LOCK mode and NORMAL mode operation.

The S2064 TTL outputs are optimized to drive 65Ω line impedance. Internal source matching provides good performance on unterminated lines of reasonable length.

Parallel Output Clock Rate

Two output clock modes are supported, as shown in Table 7. When CMODE is HIGH, a complementary TTL clock at the data rate is provided on the RCxP/N outputs. Data should be clocked on the rising edge of RCxP. When CMODE is LOW, a complementary TTL clock at 1/2 the data rate is provided. Data should be latched on the rising edge of RCxP and the rising edge of RCxN.

In Fibre Channel and Gigabit Ethernet applications, multiple consecutive K28.5 characters cannot be generated. However, for serial backplane applications this can occur. The S2064 must be able to operate properly when multiple K28.5 characters are received. After the first K28.5 is detected and aligned, the RCxP/N clock will operate without glitches or loss of cycles.

Table 7. Output Clock Mode

Mode	CMODE	RCx P/N Freq
Half Clock Mode	0	VCO/20
Full Clock Mode	1	VCO/10

OTHER OPERATING MODES

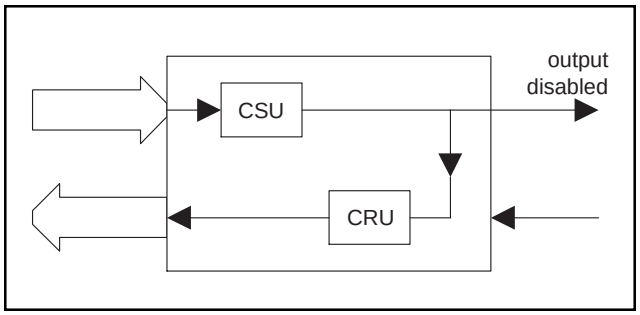
Operating Frequency Range

The S2064 is designed to operate at serial baud rates of 0.77 GHz to 1.3 GHz (800 Mbps to 1064 Mbps user data rate). The part is specified at Fibre Channel (1062 MHz) and Gigabit Ethernet (1.25 GHz) serial baud rates, but will operate satisfactorily at any rate in this range.

Loopback Mode

When loopback mode is enabled (LPEN = 1), the serial data from the transmitter is provided to the serial input of the receiver, as shown in Figure 10. This provides the ability to perform system diagnostics and off-line testing of the interface to verify the integrity of the serial channel before enabling the transmission medium. Loopback mode can be simultaneously enabled for all four channels using the loopback-enable input, LPEN. Note that the high speed outputs are disabled during loopback operation.

Figure 10. S2064 Diagnostic Loopback Operation



TEST MODES

The S2064 has a testability input to aid in functional testing of the device. The test mode is entered when CH_LOCK is HIGH and TCLKB is HIGH. Thus users must take care to insure that TCLK[B-D] are held LOW when operating in the channel locked mode. The following conditions are asserted when in test mode:

- REFCLK replaces the VCO CLK (it also still goes to the transmit clock mux).
- TCLKA clocks all 4 transmit channels.
- TCLKC is muxed in as the lock detect REFCLK for test purposes.
- TCLKD becomes the channel lock signal to the whole of the chip except the transmit clock.

The RESET pin is used to initialize the Transmit FIFOs and must be asserted (LOW) prior to entering the normal operational state (see section Transmit FIFO Initialization). Note that Reset does not disable the TCLKO output unless the TCLKB input is HIGH.

Table 8. S2064 Transmitter Input Pin Assignment and Descriptions

Pin Name	Level	I/O	Pin #	Description
DINA7 DINA6 DINA5 DINA4 DINA3 DINA2 DINA1 DINA0	TTL	I	P12 R12 T13 T12 U13 P11 R11 T11	Transmit Data for Channel A. Parallel data on this bus is clocked in on the rising edge of TCLKA or REFCLK. (See Table 1.)
SOFA	TTL	I	U15	Start of Frame A. SOFA High causes the K28.5 character of appropriate parity to be transmitted on channel A outputs. When in CHANNEL LOCK mode, SOFA High causes the K28.5 character of appropriate parity to be generated on all four channels.
KGENA	TTL	I	U14	K-Character Generation. KGENA High causes the data on DINA[0:7] to be encoded into a K-Character.
TCLKA	TTL	I	U12	Transmit Data Clock A. When TMODE is High, this signal is used to clock Data on DINA[0:7], KGENA, and SOFA into the S2064. When TMODE is Low, TCLKA is ignored.
DINB7 DINB6 DINB5 DINB4 DINB3 DINB2 DINB1 DINB0	TTL	I	R15 P14 T15 R14 U17 U16 P13 T14	Transmit Data for Channel B. Parallel data on this bus is clocked in on the rising edge of TCLKA, TCLKB, or REFCLK. (See Table 1.)
SOFB	TTL	I	R16	Start of Frame B. SOFB High causes the K28.5 character of appropriate parity to be transmitted on channel B outputs. When in CHANNEL LOCK mode, SOFB = High causes special 16 word sync character on channel x to be generated.
KGENB	TTL	I	T16	K-Character Generation. KGENB High causes the data on DINB[0:7] to be encoded into a K-Character.
TCLKB	TTL	I	R13	Transmit Data Clock B. When TMODE is High, this signal is used to clock Data on DINB[0:7], KGENB, and SOFB into the S2064. When TMODE is Low, TCLKB is ignored.
DINC7 DINC6 DINC5 DINC4 DINC3 DINC2 DINC1 DINC0	TTL	I	M15 N16 M14 R17 P16 N15 T17 N14	Transmit Data for Channel C. Parallel data on this bus is clocked in on the rising edge of TCLKA, TCLKC, or REFCLK. (See Table 1.)

Table 8. Transmitter Signal Descriptions (Continued)

Pin Name	Level	I/O	Pin #	Description
SOFC	TTL	I	N17	Start of Frame C. SOFC High causes the K28.5 character of appropriate parity to be transmitted on channel C outputs. In CHANNEL LOCK mode, SOFC is ignored.
KGENC	TTL	I	P17	K-Character Generation. KGENC High causes the data on DINC[0:7] to be encoded into a K-Character.
TCLKC	TTL	I	P15	Transmit Data Clock C. When TMODE is High, this signal is used to clock Data on DINC[0:7], KGENC, and SOFC into the S2064. When TMODE is Low, TCLKC is ignored.
DIND7 DIND6 DIND5 DIND4 DIND3 DIND2 DIND1 DIND0	TTL	I	L17 K16 K15 K14 M17 L16 M16 L15	Transmit Data for Channel D. Parallel data on this bus is clocked in on the rising edge of TCLKA, TCLKD, or REFCLK. (See Table 1.)
SOFD	TTL	I	J16	Start of Frame D. SOFD High causes the K28.5 character of appropriate parity to be transmitted on channel D outputs. In CHANNEL LOCK mode, when SOFD=Low, this resets the Channel Lock State Machine.
KGEND	TTL	I	K17	K-Character Generation. KGEND High causes the data on DIND[0:7] to be encoded into a K-Character.
TCLKD	TTL	I	L14	Transmit Data Clock D. When TMODE is High, this signal is used to clock Data on DIND[0:7], KGEND, and SOFD into the S2064. When TMODE is Low, TCLKD is ignored.

Table 9. Transmitter Output Signals

Pin Name	Level	I/O	Pin #	Description
TXAP TXAN	Diff. LVPECL	O	A17 B17	High speed serial outputs for Channel A.
TXBP TXBN	Diff. LVPECL	O	C17 D17	High speed serial outputs for Channel B.
TXCP TXCN	Diff. LVPECL	O	F16 E17	High speed serial outputs for Channel C.
TXDP TXDN	Diff. LVPECL	O	F17 G17	High speed serial outputs for Channel D.
TCLKO	TTL	O	J14	TTL Output Clock at the Parallel data rate. This clock is provided for use by up-stream circuitry.

Table 10. S2064 Mode Control Signals

Pin Name	Level	I/O	Pin #	Description
CH_LOCK	TTL	I	E4	Parallel Input Mode Control. Channel Lock High locks all four channels together. (See Table 1.)
TMODE	TTL	I	B13	Transmit Mode Control. When TMODE is Low, REFCLK is used to clock data on DINx[0:7], SOFx, and KGENx into the S2064. When TMODE is High, TCLKx is used to clock data into the S2064. In Channel Lock mode, all four channels are clocked by TCLKA. In independent mode (CH_LOCK LOW), each channel is clocked by its respective TCLK.
CLKSEL	TTL	I	C12	REFCLK Select Input. This signal configures the PLL for the appropriate REFCLK frequency. When CLKSEL = 0, the REFCLK frequency should equal the parallel word rate. When CLKSEL = 1, the REFCLK frequency should be 1/2 the parallel data rate.
REFCLK	TTL	I	H17	Reference Clock is used for the transmit VCO and frequency check for the clock recovered from the receiver serial data.
RESET	TTL	I	C15	When Low, the S2064 is held in reset. The receiver PLL is forced to lock to the REFCLK. The FIFOs are initialized on the rising edge of RESET. When High, the S2064 operates normally.
RATE	TTL	I	D12	When Low, the S2064 operates with the serial output rate equal to the VCO frequency. When High, the S2064 operates with the VCO internally divided by 2 for all functions.

Note: All TTL inputs except REFCLK have internal pull-up networks.

Table 11. S2064 Receiver Output Pin Assignment and Descriptions

Pin Name	Level	I/O	Pin #	Description
DOUTA7 DOUTA6 DOUTA5 DOUTA4 DOUTA3 DOUTA2 DOUTA1 DOUTA0	TTL	O	J1 J3 J2 H1 H2 H3 F1 G2	Channel A Receiver Data Outputs. Parallel data on this bus is valid on the rising edge of RCAP in full clock mode and valid on the rising edge of both RCAP and RCAN in half clock mode.
EOFA	TTL	O	F2	Channel A End of Frame Detected. A High on this output indicates that a valid K28.5 has been detected and is present on the parallel data outputs DOUTA[0:7].
KFLAGA	TTL	O	G3	Channel A K-Character Flag. A High in KFLAGA indicates that a valid control character has been detected. Data present on the parallel interface DOUTA[0:7] should be used to indicate which character was received.
ERRA	TTL	O	G1	Channel A Receive Error. A High on ERRA signifies the occurrence of either a parity error or an invalid codeword error during decoding of the received data.
RCAP RCAN	TTL	O	K2 K1	Receive Data Clock. Parallel receive data, DOUTA[0:7], EOFA, KFLAGA, and ERRA are valid on the rising edge of RCAP when in full clock mode and valid on the rising edge of both RCAP and RCAN in half clock mode.
DOUTB7 DOUTB6 DOUTB5 DOUTB4 DOUTB3 DOUTB2 DOUTB1 DOUTB0	TTL	O	R1 P1 M3 N2 M2 N1 L2 M1	Channel B Receiver Data Outputs. Parallel data on this bus is valid on the rising edge of RCBP in full clock mode and valid on the rising edge of both RCBP and RCBN in half clock mode.
EOFB	TTL	O	L1	Channel B End of Frame Detected. A High on this output indicates that a valid K28.5 has been detected and is present on the parallel data outputs DOUTB[0:7].
KFLAGB	TTL	O	P2	Channel B K-Character Flag. A High in KFLAGB indicates that a valid control character has been detected. Data present on the parallel interface DOUTB[0:7] should be used to indicate which character was received.
ERRB	TTL	O	K3	Channel B Receive Error. A High on ERRB signifies the occurrence of either a parity error or an invalid codeword error during decoding of the received data.
RCBP RCBN	TTL	O	U1 T1	Receive Data Clock. Parallel receive data, DOUTB[0:7], EOFB, KFLAGB, and ERRB are valid on the rising edge of RCBP when in full clock mode and valid on the rising edge of both RCBP and RCBN in half clock mode.

Table 11. S2064 Receiver Output Pin Assignment and Descriptions (Continued)

Pin Name	Level	I/O	Pin #	Description
DOUTC7 DOUTC6 DOUTC5 DOUTC4 DOUTC3 DOUTC2 DOUTC1 DOUTC0	TTL	O	R7 R6 T5 U3 T4 R5 U2 T3	Channel C Receiver Data Outputs. Parallel data on this bus is valid on the rising edge of RCCP in full clock mode and valid on the rising edge of both RCCP and RCCN in half clock mode.
EOFC	TTL	O	R2	Channel C End of Frame Detected. A High on this output indicates that a valid K28.5 has been detected and is present on the parallel data outputs DOUTC[0:7].
KFLAGC	TTL	O	P3	Channel C K-Character Flag. A High in KFLAGC indicates that a valid control character has been detected. Data present on the parallel interface DOUTC[0:7] should be used to indicate which character was received.
ERRC	TTL	O	T2	Channel C Receive Error. A High on ERRC signifies the occurrence of either a parity error or an invalid codeword error during decoding of the received data.
RCCP RCCN	TTL	O	U5 U4	Receive Data Clock. Parallel receive data, DOUTC[0:7], EOFC, KFLAGC, and ERRC are valid on the rising edge of RCCP when in full clock mode and valid on the rising edge of both RCCP and RCCN in half clock mode.
DOUTD7 DOUTD6 DOUTD5 DOUTD4 DOUTD3 DOUTD2 DOUTD1 DOUTD0	TTL	O	U11 R10 U9 R9 T9 U8 U7 T8	Channel D Receiver Data Outputs. Parallel data on this bus is valid on the rising edge of RCDP in full clock mode and valid on the rising edge of both RCDP and RCDN in half clock mode.
EOFD	TTL	O	U6	Channel D End of Frame Detected. A High on this output indicates that a valid K28.5 has been detected and is present on the parallel data outputs DOUTD[0:7].
KFLAGD	TTL	O	T7	Channel D K-Character Flag. A High in KFLAGD indicates that a valid control character has been detected. Data present on the parallel interface DOUTD[0:7] should be used to indicate which character was received.
ERRD	TTL	O	T6	Channel D Receive Error. A High on ERRD signifies the occurrence of either a parity error or an invalid codeword error during decoding of the received data.
RCDP RCDN	TTL	O	T10 U10	Receive Data Clock. Parallel receive data, DOUTD[0:7], EOFD, KFLAGD, and ERRD are valid on the rising edge of RCDP when in full clock mode and valid on the rising edge of both RCDP and RCDN in half clock mode.

Table 12. S2064 Receiver Input Pin Assignment and Descriptions

Pin Name	Level	I/O	Pin #	Description
RXAP RXAN	Diff. LVPECL	I	D4 B3	Differential LVPECL compatible inputs for channel A. RXAP is the positive input, RXAN is the negative. Internally biased to VDD-1.3V for AC coupled applications.
RXBP RXBN	Diff. LVPECL	I	C6 B5	Differential LVPECL compatible inputs for channel B. RXBP is the positive input, RXBN is the negative. Internally biased to VDD-1.3V for AC coupled applications.
RXCP RXCN	Diff. LVPECL	I	A8 A9	Differential LVPECL compatible inputs for channel C. RXCP is the positive input, RXCN is the negative. Internally biased to VDD-1.3V for AC coupled applications.
RXDP RXDN	Diff. LVPECL	I	C11 B12	Differential LVPECL compatible inputs for channel D. RXDP is the positive input, RXDN is the negative. Internally biased to VDD-1.3V for AC coupled applications.

Table 13. Receiver Control Signals

Pin Name	Level	I/O	Pin #	Description
LPEN	TTL	I	D14	Loopback Enable. When Low, input source is the high speed serial input for each channel. When High, the serial output for each channel is looped back to its input.
CMODE	TTL	I	C2	Clock Mode Control. When Low, the parallel output clocks (RCxP/N) rate is equal to 1/2 the data rate. When High, the parallel output clocks (RCxP/N) rate is equal to the data rate.

Note: All TTL inputs except REFCLK have internal pull-up networks.

Table 14. Power and Ground Signals

Pin Name	Qty.	Pin #	Description
VDDA	5	A1, A6, A13, A16, C8	Analog Power (VDD) low noise.
VSSA	5	B7, B8, B15, C4, D11	Analog Ground (VSS).
VDD	5	A12, A15, B4, B6, D9	Power for High Speed Circuitry (VDD).
VSS VSSSUB	10	A2, A4, A7, A11, A14, B10, B14, C13, D6, D8	Ground for High Speed Circuitry (VSS).

Table 14. Power and Ground Signals

Pin Name	Qty.	Pin #	Description
PECLPWR	2	E15, G16	PECL Power (VDD)
PECLGND	2	C16, H16	PECL Ground (VSS)
DIGPWR	6	B1, B2, E3, J17, L4, P9	Core Circuitry Power (VDD)
DIGGND	8	C1, C3, D2, F4, J15, N4, P10, R3	Core Circuitry Ground (VSS)
TTLPWR	8	E1, G4, H4, K4, N3, P5, P7, P8	Power for TTL I/O (VDD)
TTLGND	10	D1, E2, F3, J4, L3, M4 P4, P6, R4, R8	Ground for TTL I/O (VSS)
PWR	8	A3, B9, B11, B16, C5, C9, D7, D10	Power
GND	16	A5, A10, C7, C10, D3, D5, D15, D16, E14, E16, F14, F15, G14, G15, H14, H15	Ground
CAP1 CAP2	2	D13 C14	Pins for external loop filter capacitor

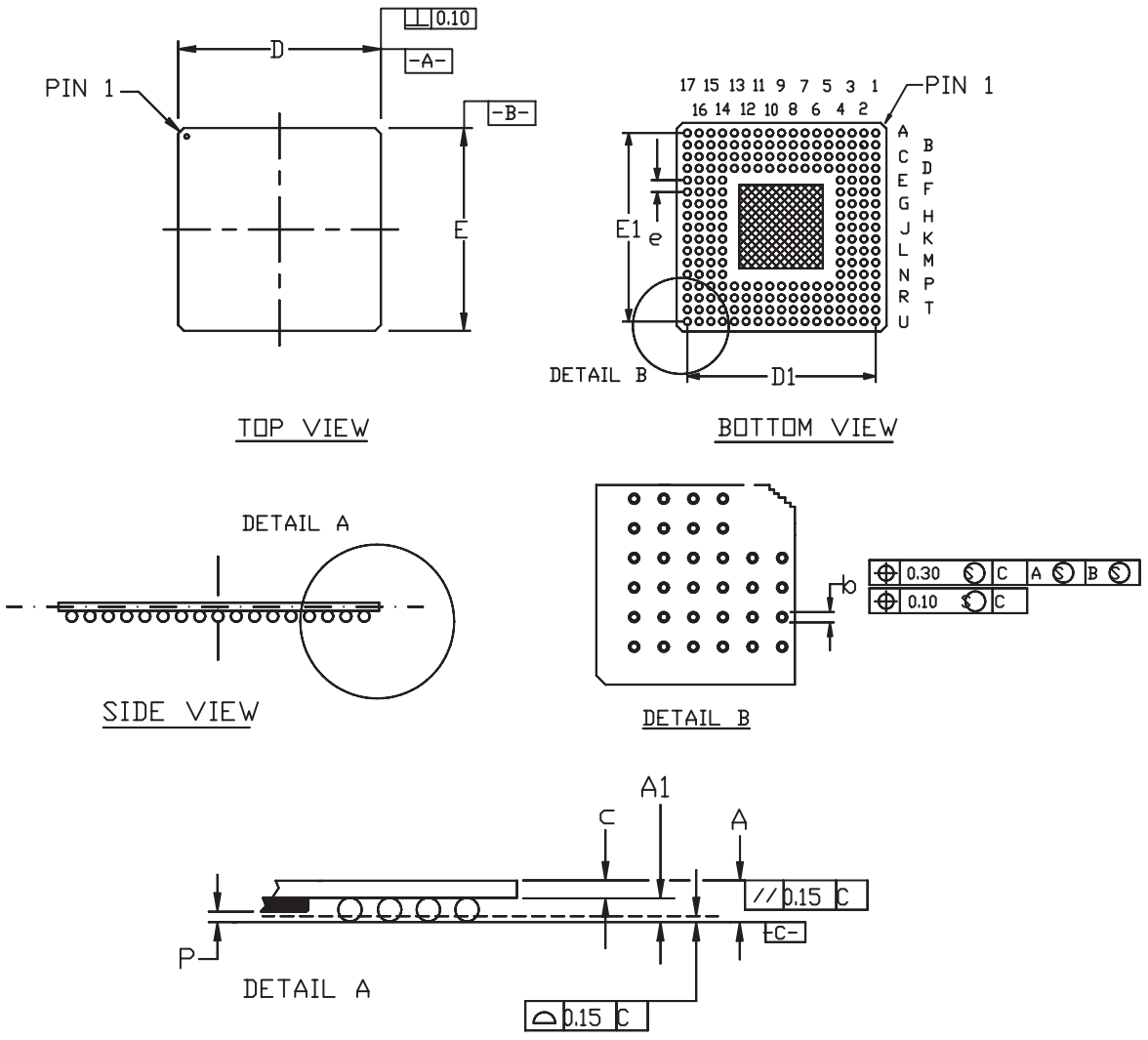
Figure 11. S2064 Pinout (Bottom View)

	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T	U
1	VDDA	DIGPWR	DIGGND	TTLGND	TTLPWR	DOUTA1	ERRA	DOUTA4	DOUTA7	RCAN	EOFB	DOUTB0	DOUTB2	DOUTB6	DOUTB7	RCBN	RCBP
2	VSSSUB	DIGPWR	CMODE	DIGGND	TTLGND	EOFA	DOUTA0	DOUTA3	DOUTA5	RCAP	DOUTB1	DOUTB3	DOUTB4	KFLAGB	EOFC	ERRC	DOUTC1
3	PWR	RXAN	DIGGND	GND	DIGPWR	TTLGND	KFLAGA	DOUTA2	DOUTA6	ERRB	TTLGND	DOUTB5	TTLPWR	KFLAGC	DIGGND	DOUTC0	DOUTC4
4	VSS	VDD	VSSA	RXAP	CH_LOCK	DIGGND	TTLPWR	TTLPWR	TTLGND	TTLPWR	DIGPWR	TTLGND	DIGGND	TTLGND	TTLGND	DOUTC3	RCCN
5	GND	RXBN	PWR	GND										TTLPWR	DOUTC2	DOUTC5	RCCP
6	VDDA	VDD	RXBP	VSS										TTLGND	DOUTC6	ERRD	EOFD
7	VSSSUB	VSSA	GND	PWR										TTLPWR	DOUTC7	KFLAGD	DOUTD1
8	RXCP	VSSA	VDDA	VSSSUB										TTLPWR	TTLGND	DOUTD0	DOUTD2
9	RXCN	PWR	PWR	VDD										DIGPWR	DOUTD4	DOUTD3	DOUTD5
10	GND	VSS	GND	PWR										DIGGND	DOUTD6	RCDP	RCDN
11	VSS	PWR	RXDP	VSSA										DINA2	DINA1	DINA0	DOUTD7
12	VDD	RXDN	CLKSEL	RATE										DINA7	DINA6	DINA4	TCLKA
13	VDDA	TMODE	VSSSUB	CAP1										DINB1	TCLKB	DINA5	DINA3
14	VSSSUB	VSS	CAP2	LPEN	GND	GND	GND	GND	TCLKO	DIND4	TCLKD	DINC5	DINC0	DINB6	DINB4	DINB0	KGENA
15	VDD	VSSA	RESET	GND	PECL PWR	GND	GND	GND	DIGGND	DIND5	DIND0	DINC7	DINC2	TCLKC	DINB7	DINB5	SOFA
16	VDDA	PWR	PECLGND	GND	GND	TXCP	PECL PWR	PECLGND	SOFD	DIND6	DIND2	DIND1	DINC6	DINC3	SOFB	KGENB	DINB2
17	TXAP	TXAN	TXBP	TXBN	TXCN	TXDP	TXDN	REFCLK	DIGPWR	KGEND	DIND7	DIND3	SOFC	KGENC	DINC4	DINC1	DINB3

Figure 12. S2064 Pinout (Top View)

	U	T	R	P	N	M	L	K	J	H	G	F	E	D	C	B	A
1	RCBP	RCBN	DOUTB7	DOUTB6	DOUTB2	DOUTB0	EOFB	RCAN	DOUTA7	DOUTA4	ERRA	DOUTA1	TTLPWR	TTLGND	DIGGND	DIGPWR	VDDA
2	DOUTC1	ERRC	EOFC	KFLAGB	DOUTB4	DOUTB3	DOUTB1	RCAP	DOUTA5	DOUTA3	DOUTA0	EOFA	TTLGND	DIGGND	CMODE	DIGPWR	VSSSUB
3	DOUTC4	DOUTC0	DIGGND	KFLAGC	TTLPWR	DOUTB5	TTLGND	ERRB	DOUTA6	DOUTA2	KFLAGA	TTLGND	DIGPWR	GND	DIGGND	RXAN	PWR
4	RCCN	DOUTC3	TTLGND	TTLGND	DIGGND	TTLGND	DIGPWR	TTLPWR	TTLGND	TTLPWR	TTLPWR	DIGGND	CH_LOCK	RXAP	VSSA	VDD	VSS
5	RCCP	DOUTC5	DOUTC2	TTLPWR										GND	PWR	RXBN	GND
6	EOFD	ERRD	DOUTC6	TTLGND										VSS	RXBP	VDD	VDDA
7	DOUTD1	KFLAGD	DOUTC7	TTLPWR										PWR	GND	VSSA	VSSSUB
8	DOUTD2	DOUTD0	TTLGND	TTLPWR										VSSSUB	VDDA	VSSA	RXCP
9	DOUTD5	DOUTD3	DOUTD4	DIGPWR										VDD	PWR	PWR	RXCN
10	RCDN	RCDP	DOUTD6	DIGGND										PWR	GND	VSS	GND
11	DOUTD7	DINA0	DINA1	DINA2										VSSA	RXDP	PWR	VSS
12	TCLKA	DINA4	DINA6	DINA7										RATE	CLKSEL	RXDN	VDD
13	DINA3	DINA5	TCLKB	DINB1										CAP1	VSSSUB	TMODE	VDDA
14	KGENA	DINB0	DINB4	DINB6	DINC0	DINC5	TCLKD	DIND4	TCLKO	GND	GND	GND	GND	LPEN	CAP2	VSS	VSSSUB
15	SOFA	DINB5	DINB7	TCLKC	DINC2	DINC7	DIND0	DIND5	DIGGND	GND	GND	GND	PECL PWR	GND	RESET	VSSA	VDD
16	DINB2	KGENB	SOFB	DINC3	DINC6	DIND1	DIND2	DIND6	SOFD	PECLGND	PECL PWR	TXCP	GND	GND	PECLGND	PWR	VDDA
17	DINB3	DINC1	DINC4	KGENC	SOFC	DIND3	DIND7	KGEND	DIGPWR	REFCLK	TXDN	TXDP	TXCN	TXBN	TXBP	TXAN	TXAP

Figure 13. Compact 23mm x 23mm 208 TBGA Package



DIMENSIONS (are in millimeters)

UNIT	A	A_1	D	D_1	E	E_1	P	b	c	e
MIN	1.45	0.60	22.80	20.32 BSC.	22.80	20.32 BSC.		0.65	0.85	1.27 BSC.
NOM	1.55	0.65	23.00		23.00			0.75	0.90	
MAX	1.65	0.70	23.20		23.20		0.25	0.85	0.95	

Thermal Management

Device	Θja (Still Air)	Θjc
S2064	17.7° C/W	3.5° C/W

Figure 14. Transmitter Timing (Normal or Channel Lock Mode, TMODE = 0)

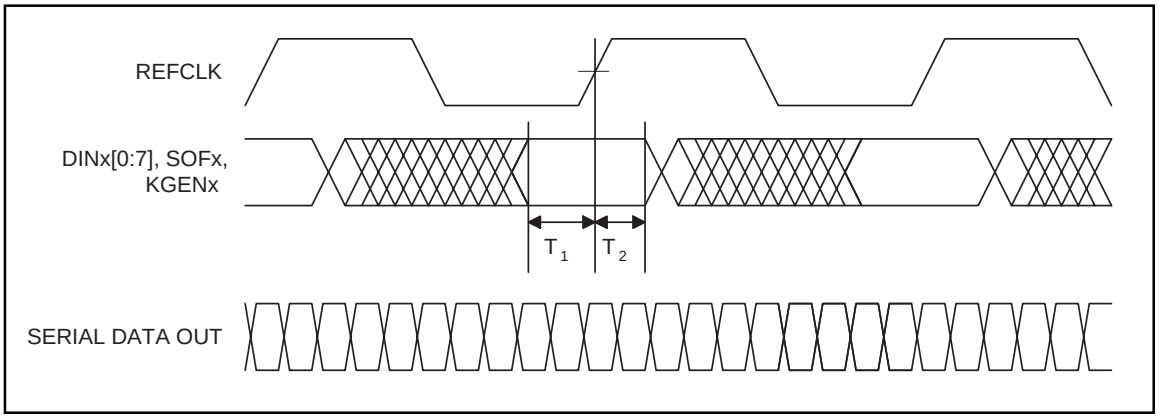


Table 15. S2064 Transmitter Timing (Normal or Channel Lock Mode, TMODE = 0)

Parameters	Description	Min	Max	Units	Conditions
T_1	Data Setup w.r.t. ↑ REFCLK	0.5	-	ns	See Note 1.
T_2	Data Hold w.r.t. ↑ REFCLK	1.3	-	ns	

1. All AC measurements are made from the reference voltage levels of the clock (1.4V) to the valid input or output data levels (.8V or 2.0V).

Figure 15. Transmitter Timing (Normal or Channel Lock Mode, TMODE = 1)

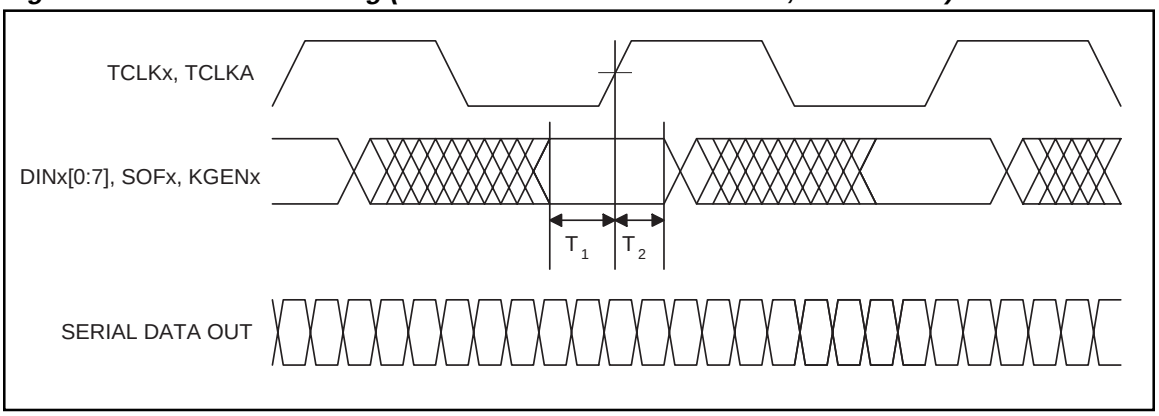


Table 16. S2064 Transmitter Timing (Normal or Channel Lock Mode, TMODE = 1)

Parameters	Description	Min	Max	Units	Conditions
T_1	Data Setup w.r.t. ↑ TCLK	1.0	-	ns	See Note 1.
T_2	Data Hold w.r.t. ↑ TCLK	0.5	-	ns	

1. All AC measurements are made from the reference voltage levels of the clock (1.4V) to the valid input or output data levels (.8V or 2.0V).

Figure 16. Receiver Timing (Full Clock Mode, CMODE = 1)

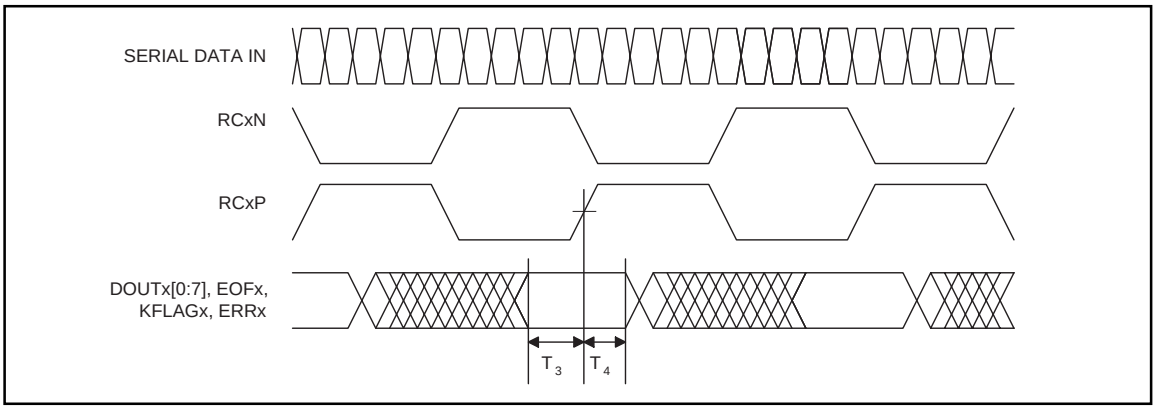


Figure 17. Receiver Timing (Half Clock Mode, CMODE = 0)

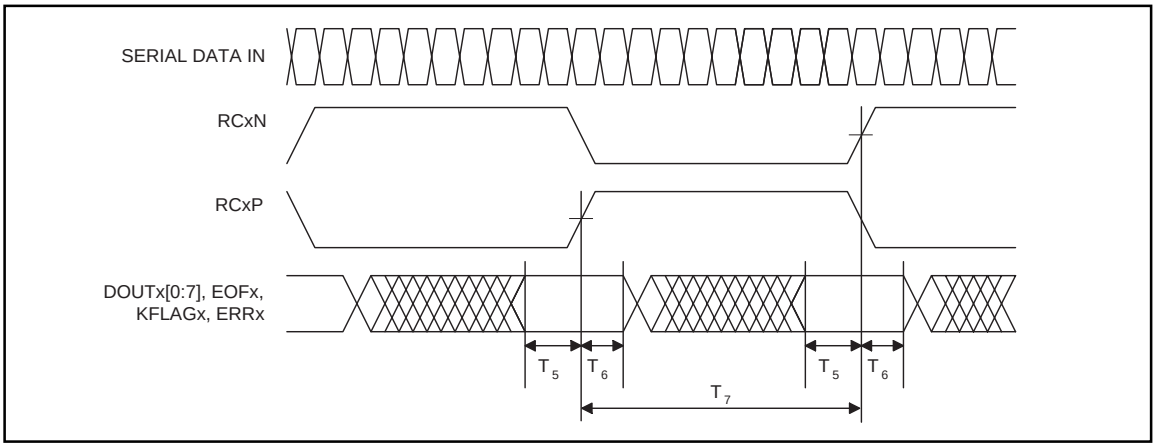


Table 17. S2064 Receiver Timing (Full and Half Clock Mode)

Parameters	Description	Min	Max	Units	Conditions
T_3	Data Setup w.r.t. ↑RCxP/N	2.75 3.5		ns	at 1.25 Gbps at 1.062 Gbps[1]
T_4	Data Hold w.r.t. ↑RCxP/N	2.0		ns	
T_5	Data Setup w.r.t. ↑RCxP/N	2.5 3.5		ns	at 1.25 Gbps at 1.062 Gbps[1]
T_6	Data Hold w.r.t. ↑RCxP/N	2.0		ns	
T_7	Time from RCxP rise to RCxN rise	7.8 9.3	8.82 10.4	ns ns	at 1.25 Gbps at 1.062 Gbps[1]
T_{RP}, T_{FP}	RCxP Rise and Fall Times		3.0	ns	See Figure 20.
T_{RN}, T_{FN}	RCxN Rise and Fall Times		3.0	ns	See Figure 20.
T_{DR}, T_{DF}	DOUTx Rise and Fall Times		3.0	ns	See Figure 19.
Duty Cycle	RCLK Duty Cycle	40	60	%	

1. Measurements made from the reference voltage levels of the clock (1.4V) to the valid input or output data levels (.8V or 2.0V).

Figure 18. TCLKO Timing

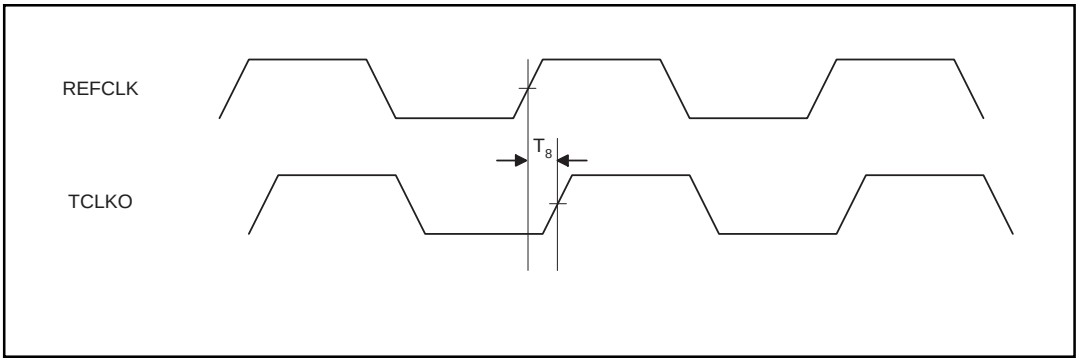


Table 18. S2064 Transmitter (TCLKO Timing)

Parameters	Description	Min	Max	Units	Conditions
T_8	TCLKO↑ w.r.t.↑ REFCLK	2	7.5	ns	
TCLKO Duty Cycle		40%	60%	%	

Note: Measurements are made at 1.4V level of clocks.

Table 19. Absolute Maximum Ratings

Parameter	Min	Typ	Max	Units
Case Temperature Under Bias	-55		125	˚C
Junction Temperature Under Bias	-55		150	˚C
Storage Temperature	-65		150	˚C
Voltage on VDD with Respect to GND	-0.5		+7.0	V
Voltage on any TTL Input Pin	-0.5		3.47	V
Voltage on any PECL Input Pin	0		VDD	V
TTL Output Sink Current			8	mA
TTL Output Source Current			8	mA
High Speed PECL Output Source Current			30	mA
Static Discharge Voltage, TTL I/O		2000*		V
Static Discharge Voltage, PECL I/O		1500		V

*All TTL pins are rated at 2 kV except for pins G3 and J14.

Table 20. Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
Ambient Temperature Under Bias	0		70	˚C
Junction Temperature Under Bias			130	˚C
Voltage on any Power Pin with Respect to GND/VSS	3.13	3.3	3.47	V
Voltage on any TTL Input Pin	0		3.47	V
Voltage on any PECL Input Pin	VDD -2V		VDD	V

Table 21. Reference Clock Requirements

Parameters	Description	Min	Max	Units	Conditions
FT	Frequency Tolerance	-100	+100	ppm	
TD_{1-2}	Symmetry	40	60	%	Duty Cycle at 50% pt.
T_{RCR}, T_{RCF}	REFCLK Rise and Fall Time		2	ns	20% - 80%.
—	Jitter		80	ps	Peak-to-Peak, to maintain ≥77% eye opening.

Table 22. Serial Data Timing, Transmit Outputs

Parameters	Description	Min	Typ	Max	Units	Comments
Total Jitter	Serial Data Output total jitter			192	ps	Peak-to-Peak.
T_{DJ}	Serial Data Output deterministic jitter			80	ps	Peak-to-Peak.
T_{SR}, T_{SF}	Serial Data Output rise and fall time			300	ps	20% - 80%. 4.5 kΩ to ground.

Table 23. Serial Data Timing, Receive Inputs

Parameters	Description	Min	Typ	Max	Units	Comments
T_{LOCK} (Frequency)	Frequency Acquisition Lock Time (Loss of Lock) (1.25 Gbps)	–	–	175	µs	8B/10B idle pattern sample basis, from device start up.
T_{LOCK} (Phase)	Phase Acquisition Lock Time (Phase Discontinuity) (1.25 Gbps)	–	–	150	ns	90% Input data eye (See Figure 24).
		_	–	180	ns	70% Input data eye.
T_{DJ}	Deterministic Input Jitter Tolerance	370	–	–	ps	
Input Jitter Tolerance	Serial Data Input total jitter tolerance	599	–	–	ps	Peak-to-Peak, as specified by IEEE 802.3z.
R_{SR}, R_{SF}	Serial Data Input rise and fall time	–	–	350	ps	20% - 80%.

Table 24. DC Characteristics

Parameters	Description	Min	Typ	Max	Units	Conditions
V_{OH}	Output High Voltage (TTL)	2.4	2.8	VDD	V	VDD = min I_{OH} = -4mA
V_{OL}	Output Low Voltage (TTL)	GND	.025	0.5	V	VDD = min I_{OL} = 4mA
V_{IH}	Input High Voltage (TTL)	2.0			V	
V_{IL}	Input Low Voltage (TTL)	GND		0.8	V	
I_{IH}	Input High Current (TTL)			40	µA	V_{IN} = 2.4 V, VDD = Max
I_{IL}	Input Low Current (TTL)			600	µA	V_{IN} = 0.8 V, VDD = Max
IDD	Supply Current		750	920	mA	1010 Pattern.
P_D	Power Dissipation		2.3	3.15	W	1010 Pattern.
V_{DIFF}	Min. differential input voltage swing for differential PECL inputs	100		2200	mV	See Figure 22.
ΔV_{OUT}	Differential Serial Output Voltage Swing	1200	1900	2200	mV	AC coupled with 4.5 kΩ pulldown and 100 Ω differential termination. See Figure 21.
C_{IN}	Input Capacitance			3	pf	

OUTPUT LOAD

The S2064 serial outputs require a resistive load to set the output current. The recommended resistor value is 4.5 kΩ to ground. This value can be varied to adjust drive current, signal voltage swing, and power usage on the board.

ACQUISITION TIME

With the input eye diagram shown in Figure 24, the S2064 will recover data with a ≤10E-9 BER within the time specified by T_{LOCK} in Table 23 after an instantaneous phase shift of the incoming data.

Figure 19. Serial Input/Output Rise and Fall Time

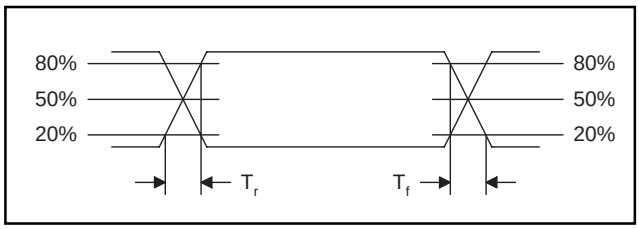


Figure 20. TTL Input/Output Rise and Fall Time

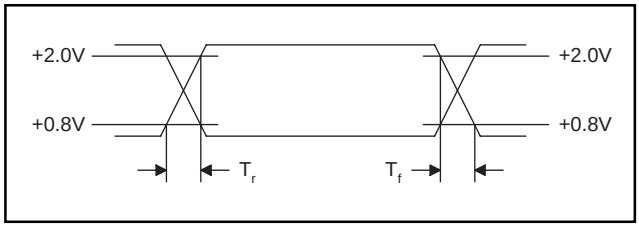


Figure 21. Serial Output Load

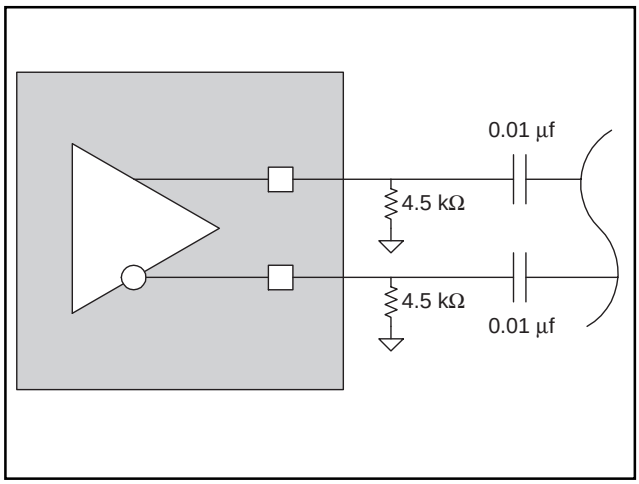


Figure 22. High Speed Differential Inputs

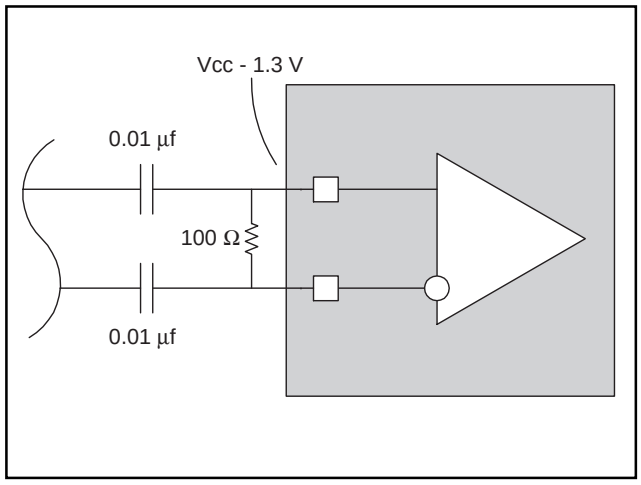


Figure 23. Receiver Input Eye Diagram Jitter Mask

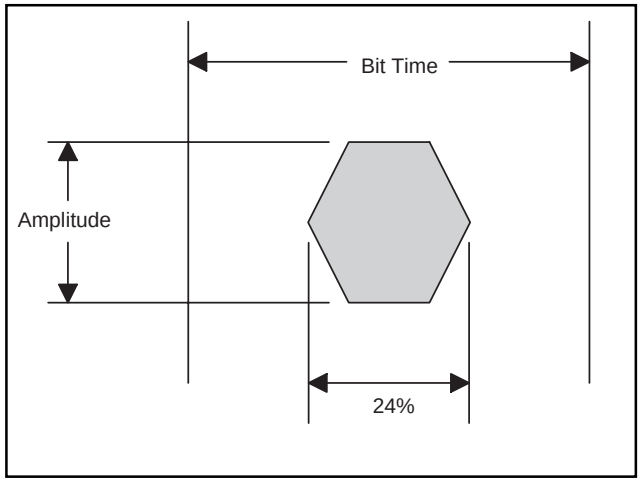


Figure 24. Acquisition Time Eye Diagram

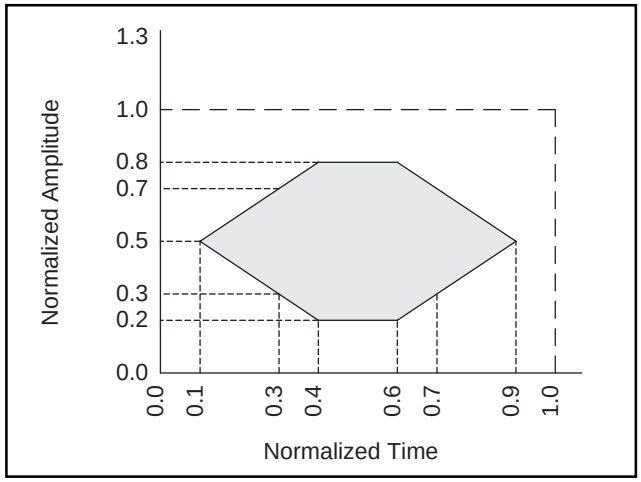
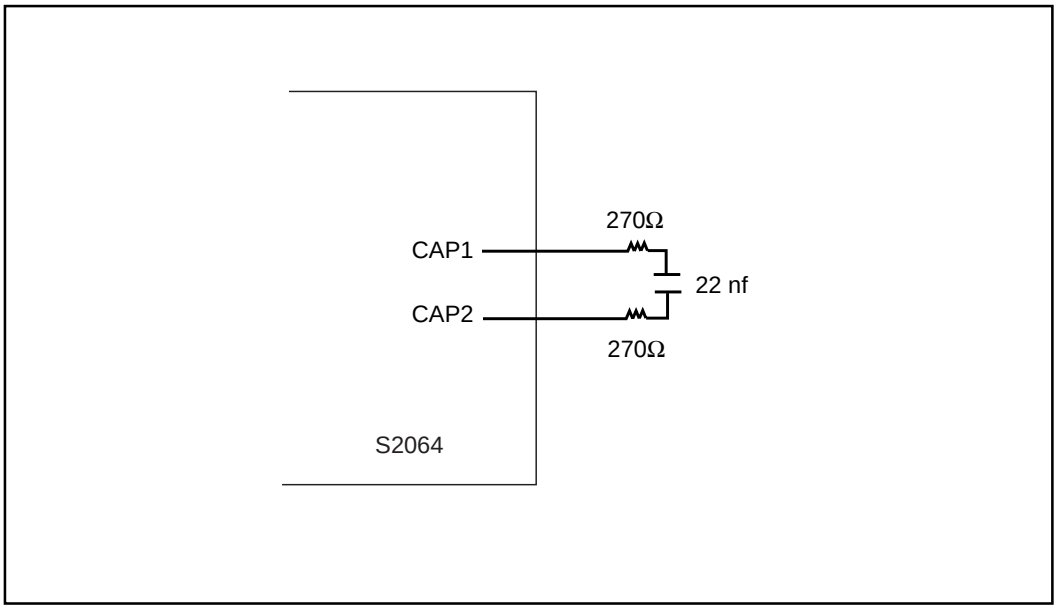
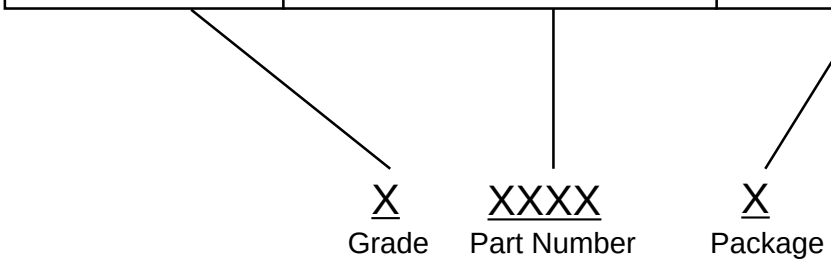


Figure 25. Loop Filter Capacitor Connections



Ordering Information

Grade	Part No.	Package
S – Commercial	S2064	A – 208 TBGA



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